REMARKS

Claims 1-53, 55-90 and 92-110 are now pending in the application. Support for the amendments to the claims can be found throughout the drawings and specification. As such, no new matter is added. Further, Applicants respectfully submit that the amendments clarify subject matter that was already implicit in the claims as recited. As such, no new issues are raised. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 1, 12, 24, 37, 48, 61, 74, 85, and 98 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dankberg (U.S. Pat. No. 5,596,439) and He (U.S. Pat. No. 6,870,881) and further in view of Rabenko et al. (U.S. Pat. No. 6,765,931). This rejection is respectfully traversed.

With respect to claim 1, Dankberg, either singly or in combination with He and Rabenko, fails to show, teach, or suggest at least that the composite signal, the replica transmission signal, and the analog baseline correction current are **directly connected together at a common node** of the first sub-circuit.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, the alleged combination fails to disclose the limitation

that the composite signal, the replica transmission signal, and the analog baseline correction current are **directly connected together at a common node**.

As shown in an exemplary embodiment in FIG. 11 of the present application, an active resistive summer (i.e. a first sub-circuit) includes an operational amplifier with a negative input terminal. The negative input terminal receives, as inputs, a composite signal V_{txRL}, a replica signal V_{txR}, and an analog baseline correction current I_{bl}. Each of the composite signal V_{txRL}, the replica signal V_{txR}, and the analog baseline correction current I_{bl} are connected together at the negative input terminal. In other words, the signals are **directly connected together at a common node of the first sub-circuit**.

The Examiner acknowledges that Dankberg fails to disclose that the composite signal, the replica transmission signal, and the baseline correction current are connected together at a common node and instead relies on He to disclose this limitation. In particular, the Examiner alleges that FIG. 9 of He discloses an adder 22 that "receives signals from echo canceller 10 and baseline correction circuit 12." Applicants respectfully note that **He still fails to disclose that the three signals are directly connected together at a common node**.

For example, a different adder 14 receives an output from the baseline correction circuit 12. This output is combined with another signal and input to ADC 16. The ADC 16 outputs a digital signal to delay adjustment block 20. An output of the delay adjustment block 20 is received at the adder 22. As such, Applicants respectfully assert that **the output of the baseline correction circuit is not directly connected together at a common node with the composite signal and the replica transmission signal**.

In response, the Examiner alleges that a baseline correction current from element 12 "eventually makes its way to adder 22." Applicants respectfully disagree and notes that this current is never input to adder 22 and is instead input to adder 14. The output of adder 22 is no longer a baseline correction current.

For example, the adder 14 receives input signals from Ethernet cable 6. The adder 14 also receives "correction signals supplied from baseline wander correction block 12." (See Column 5, Lines 7-9). These correction signals are added to the input signals. In other words, the output of the adder 14 is merely an adjusted version of the input signals from the Ethernet cable 6. As such, the Examiner's assertion that the output of the adder 14 is, or include, a baseline wander correct current is patently improper.

Further, the output from the adder 14 is then received by analog-to-digital converter (ADC) 16 and converted to a digital signal. Applicants respectfully note that a digital signal is neither a baseline correction current nor includes a baseline correction current. Here again, Applicants submit that this intermediate signal is not a baseline correction current. In particular, **a signal that is previously adjusted by a correction current does is not properly interpreted as the correction current at another stage of a circuit**.

Applicants respectfully note that Dankberg fails to disclose that the three signals are directly connected together at a common node. As described above, He fails to make up for the deficiencies of Dankberg and is absent of any teaching or suggestion of directly connecting the signals together at a common node. As such, combining Dankberg with He and/or Rabenko still fails to disclose the elements of claim 1.

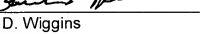
Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 12, 24, 37, 48, 61, 74, 85, and 98, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: February 19, 2008

By: 

Michael D. Wiggins
Reg. No. 34,754

Damian M. Aquino
Reg. No. 54,964

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/DMA/dms